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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/755,734	01/12/2004	Roger D. Isaac	5500-91000	1103

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EXAMINER	
KIM, DANIEL Y	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 09/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/755,734	ISAAC ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed June 26, 2006 in response to the PTO Office Action mailed March 16, 2006. The applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, claims 1-3, 10-11, and 18-26 have been amended, and no claims have been cancelled or added. Claims 1-26 remain pending in this application.

3. The objections to claims 3 and 18-25 have been withdrawn due to the amendment filed June 26, 2006.

Response to Arguments

4. Applicant's arguments with respect to claim have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3, 9-12, 18-20 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehrotra et al (US Patent No. 6,145,054) and Gruner et al (US PGPub No. 20030154346).

For claim 1, Mehrotra discloses a cache memory subsystem comprising:

a cache storage configured to store a plurality of cache lines of data (a pipelined hierarchical cache system, col. 2, line 65).

Mehrotra fails to disclose the remaining claim limitations.

Gruner, however, helps disclose a scheduler configured to schedule reads and writes of information to said cache storage using a pipeline (as described by Mehrotra above) with a fixed latency (a cache includes a scheduler for assigning priority to memory requests; the scheduler also selects a request entry before it remains in a queue for a predetermined period of time, par. 0117; the scheduler assigns priority to memory requests based on predetermined criteria; in one embodiment, the predetermined criteria are programmable, par. 0118; if the requested operation is a store, the cache performs a read-modify-write operation wherein the cache supplies the addressed cache line to a store buffer; the cache modifies the cache line addresses by a first tier memory request; the cache then forwards the contents, making this transfer once the cache has an idle cycle or a predetermined period of time elapses, par. 0131);

wherein in response to scheduling a read request to said cache storage, said scheduler is further configured to cause an associated write to said cache storage to occur a fixed number of cycles after scheduling a read request (par. 0117-0118, 0131).

Mehrotra and Gruner are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a scheduler for scheduling reads and writes of information to a cache in a fixed latency pipeline because this prioritization process would help to review and identify operations (par. 0119), as taught by Gruner.

For claim 2, the combined teachings of Mehrotra and Gruner disclose the invention as per rejection of claim 1.

These teachings further help disclose said associated write corresponds to a cache line of victim data which has been evicted from a higher-level cache in response to a read miss of said higher-level cache (Mehrotra: detecting if a first instruction generates a first cache miss, and marking the first cache miss as a primary reference, and a servicing step services the first cache miss with a line of data, col. 3, lines 54-57; a victim queue communicates with the miss queue and the write queue for read and write misses, col. 18, lines 40-42; Gruner: a second tier cache accesses a first tier cache to provide fill data when the first tier cache has a miss, par. 0096).

For claim 3, the combined teachings of Mehrotra and Gruner disclose the invention as per rejection of claim 2.

Gruner further helps disclose said scheduler is further configured to perform said associated write to a storage location within said cache storage having an address corresponding to said cache line of victim data (the cache includes memory request queues for receiving and maintaining memory requests from data caches; each queue entry contains a memory request descriptor, including an address field, par. 0114).

For claim 9, the combined teachings of Mehrotra and Gruner disclose the invention as per rejection of claim 1 above.

Mehrotra further helps disclose a tag storage configured to store a plurality of tags each corresponding to a respective cache line of said plurality of cache lines (each cache has a tag array for storing tags to the cache, and a data array for storing the data of the cache, col. 9, lines 50-51).

For claim 10, the combined teachings of Mehrotra and Gruner disclose the invention as per rejection of claim 1 above.

These teachings further disclose a method for use with the system described as in claim 1 (Mehrotra: the present invention involves a method and apparatus for a non-blocking hierarchical cache distributed over multiple levels, col. 5, lines 44-46; Gruner: a multi-processor unit in accordance with the present invention, par. 0032; a process employed by the multi-processor unit to exchange data in accordance with the present invention, par. 0033).

Claim 11 is rejected using the combined rationale as in the rejections of claims 2 and 10 above.

Claim 12 is rejected using the combined rationale as in the rejections of claims 3 and 11 above.

For claim 18, the combined teachings of Mehrotra and Gruner disclose the invention as per rejection of claim 1 above.

These teachings further help disclose a microprocessor comprising:

an execution unit configured to execute instructions and operate on data (Mehrotra: a hierarchical cache memory using multiple levels of non-blocking caches having distributed control in a microprocessor, col. 1, lines 24-27);

a higher-level cache memory subsystem coupled to store a first plurality of cache lines of said data in a first cache storage (Mehrotra: a data cache memory unite including a cache memory comprises two hierarchical levels of cache memory on-chip, L1$ and L2$, col. 8, lines 45-50);

a lower-level cache subsystem coupled to said higher-level cache subsystem, wherein said lower-level cache subsystem includes:

a second cache storage configured to store a second plurality of cache lines of said data (Mehrotra: col. 8, lines 45-50);

a scheduler configured to schedule reads and writes of information to said second cache storage using a fixed latency pipeline (Gruner: par. 0117-0118);

wherein in response to scheduling a read request from said higher-level cache subsystem, said scheduler is further configured to cause an associated write to said second cache storage to occur a fixed number of cycles after said scheduling a read request (par. 0117-118; 0131).

Claim 19 is rejected using the combined rationale as in the rejections of claims 2 and 18 above.

Claim 20 is rejected using the combined rationale as in the rejections of claims 3 and 19 above.

Claim 26 is rejected using the combined rationale as in the rejection of claim 18 above.

7. Claims 4-5, 13-14 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehrotra et al (US Patent No. 6,145,054), Gruner et al (US PGPub No. 20030154346) and Flynn (US Patent No. 6,345,335).

For claim 4, the combined teachings of Mehrotra and Gruner disclose the invention as per rejection of claim 1.

These teachings fail to disclose the limitations of claim 4.

Flynn, however, helps disclose an associated write corresponds to a cache line of fill data from a system memory (when a miss occurs and a line fill operation is requested, the memory controller can request the address data words or instruction words from main memory; line fill data words are returned from the main memory, col. 5, lines 29-36).

Mehrotra, Gruner and Flynn are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include writing a cache line of fill data from a system memory because this is a benefit of a

design in which a cache is connected to a memory controller coupled to a data address buss and instruction address bus (col. 5, lines 20-32), as taught by Flynn.

Claim 5 is rejected using the combined rationale as for the rejections of claims 3-4 above.

Claim 13 is rejected using the combined rationale as in the rejections of claims 4 and 10 above.

Claim 14 is rejected using the combined rationale as in the rejections of claims 5 and 14 above.

Claim 21 is rejected using the combined rationale as in the rejections of claims 4 and 18 above.

Claim 22 is rejected using the combined rationale as in the rejections of claims 5 and 19 above.

8. Claims 6-8, 15-17 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehrotra et al (US Patent No. 6,145,054), Gruner et al (US PGPub No. 20030154346) and Rowlands (US PGPub No. 20030217236).

For claim 6, the combined teachings of Mehrotra and Gruner disclose the invention as per rejection of claim 1.

These teachings fail to disclose the limitations of claim 6.

Rowlands, however, helps disclose in response to scheduling said read request, said scheduler is further configured to provide an indication that said read request is scheduled and that a read response will follow (a requesting agent in a node initiates a

transaction to a cache block for which another node is the home node, par. 0110; transactions on the interconnect in a given node may involve an address phase, a response phase, and a data phase for read and write transactions; the address phase is transmitted by the initiator of the transaction, and includes the address of the affected cache block, the type of transaction, and other control information; the response phase occurs after the address phase, and indicates the ownership of other agents within the node; in one embodiment, the response phase occurs at a predetermined delay from the corresponding address phase; the predetermined delay may be programmable or fixed in various embodiments, par. 0109; the requesting agent drives the address phase on the interconnect, and the address phase is detected by the memory bridge; the response phase occurs, transferring exclusive ownership within the node to the requesting agent, par. 0110; fig. 1, items 10, 22, 36).

Mehrotra, Gruner and Rowlands are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include providing a read response and an indication of such to a read request because this would help to indicate intranode ownership of a cache block or line (par. 0109), especially in distributed memory systems for maintaining cache coherency (par. 0003), as taught by Rowlands.

For claim 7, the combined teachings of Mehrotra, Gruner and Rowlands disclose the invention as per rejection of claim 6 above.

Rowlands further helps disclose said scheduler is further configured to provide said indication a predetermined amount of time before said read response (par. 0109).

For claim 8, the combined teachings of Mehrotra, Gruner and Rowlands disclose the invention as per rejection of claim 7 above.

Rowlands further helps disclose said predetermined amount of time is programmable (par. 0109).

Claim 15 is rejected using the combined rationale as in the rejections of claims 6 and 10 above.

Claim 16 is rejected using the combined rationale as in the rejections of claims 7 and 15 above.

Claim 17 is rejected using the combined rationale as in the rejections of claims 8 and 16 above.

Claim 23 is rejected using the combined rationale as in the rejections of claims 6 and 18 above.

Claim 24 is rejected using the combined rationale as in the rejections of claims 7 and 23 above.

Claim 25 is rejected using the combined rationale as in the rejections of claims 8 and 24 above.

Citation of Pertinent Prior Art

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hetherington et al (US Patent No. 6,154,812) discloses a data cache unit associated with a processor, including a second non-blocking cache for servicing misses in a first non-blocking cache.

Gwilt et al (US PGPub No. 20040024974) discloses a cache controller comprising a linefill mechanism.

Contact Information

10. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 10:00am-6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah, is also reachable at 571-272-4098.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

8-28-06

SANJIV SHAH
PRIMARY EXAMINER